REMARKS

This is in response to the Office Action mailed on February 18, 2005, and for which a three-month extension is hereby requested. The Office Action rejected claims 63-77 and 80-124 for failing to comply with 37 CFR §41.202(a). It is believed that the various requirements of this rule have been met previously prior to the introduction of this rule; however, to comply with the Office Action, this material is re-presented below in the format specified by the rule.

Consequently, in response to the various portions of 37 CFR §41.202(a):

(1) Identification of Patent

Section (1) requires sufficient information to identify the patents with which the interference is sought.

Claims 63-77 are substantial copies claims 1, 3, 4, 6, 13, 15-17, 19, 20, and 29-33, respectively, of U.S. Patent No. 6,014,327 of Banks, granted issue January 11, 2000. Claims 63-72 are also substantial copies of claims 7, 9, 10, 12, 21, 23-25, 27, and 28, respectively, of the Banks `486 patent.

Claims 80-93 are substantial copies claims 1-6 and 13-20, respectively, of U.S. Patent No. 6,356,486 of Banks, granted issue March 12, 2002. Claims 80-93 are also substantial copies of claims 7-12, and 21-28, respectively, of the Banks `486 patent.

Claims 94-98, 100, 102, 104, and 106 are exact copies of claims 1, 3-6, 12, 15, 18, and 21, respectively, of U.S. Patent No. 6,381,172 of Banks, issued April 30, 2002. Claims 99, 101, 103, and 105 are substantial copies of the pairs of claims 7 and 8, 13 and 14, 16 and 17, and 19 and 20, respectively, of U.S. Patent No. 6,381,172.

Claims 107-109, 111, 113-115, 117, 119-121, and 123 are exact copies of claims 1-3, 6, 9-11, 14, 17-19, and 22, respectively, of U.S. Patent No. 6,404,675 of Banks, issued June 11, 2002. Claims 110, 112, 116, 118, 122, and 124 are substantial copies of the pairs of claims 4 and 5, 7 and 8, 12 and 13, 15 and 16, 20 and 21, and 23 and 24, respectively, of U.S. Patent No. 6,404,675.

(2) Identification of Claims Believed to Interfere, ProposedCount, and Claim Correspondence

Section (2) requires that all claims believed to interfere are identified, that one or more counts is proposed, and that it is shown how the claims correspond to the one or more counts.

Claims 63-72 are substantial copies claims 1, 3, 4, 6, 13, 15-17, 19, and 20, respectively, and of claims 7, 9, 10, 12, 21, 23-25, 27, and 28, respectively, of U.S. Patent No. 6,014,327 and, consequently, so correspond.

Claims 73-77 are substantial copies claims 29-33, respectively, of U.S. Patent No. 6,014,327 and, consequently, so correspond.

Claims 80-93 are substantial copies claims 1-6 and 13-20, respectively, and of of claims 7-12, and 21-28, respectively, of U.S. Patent No. 6,356,486 and, consequently, so correspond.

Claims 94-98, 100, 102, 104, and 106 are exact copies of claims 1, 3-6, 12, 15, 18, and 21, respectively, of U.S. Patent No. 6,381,172 and, consequently, so correspond.

Claims 99, 101, 103, and 105 are substantial copies of the pairs of claims 7 and 8, 13 and 14, 16 and 17, and 19 and 20, respectively, of U.S. Patent No. 6,381,172 and, consequently, so correspond.

Claims 107-109, 111, 113-115, 117, 119-121, and 123 are exact copies of claims 1-3, 6, 9-11, 14, 17-19, and 22, respectively, of U.S. Patent No. 6,404,675 and, consequently, so correspond.

Claims 110, 112, 116, 118, 122, and 124 are substantial copies of the pairs of claims 4 and 5, 7 and 8, 12 and 13, 15 and 16, 20 and 21, and 23 and 24, respectively, of U.S. Patent No. 6,404,675 and, consequently, so correspond.

Claim 63 of the present application, which is a substantial copy of both claims 1 and 7 of U.S. Patent No. 6,014,327 is suggested as a Count 1:

<u>Count 1</u>

For an electrically alterable non-volatile multi-level memory device including a plurality of non-volatile multi-level memory cells, each of the multi-level memory cells including a floating gate FET having a channel with electrically alterable voltage threshold value, the plurality of non-volatile multi-level memory cells being disposed in a matrix of rows and columns, channels of multi-level memory cells of a first group of the plurality of non-volatile multi-level memory cells being coupled in parallel between a first bit line and a reference potential, channels of multi-level memory cells of a second group of the plurality of non-volatile multi-level memory cells being coupled in parallel between a second bit line and the reference potential, electrons being capable of being injected into the floating gate from the channel of each of the plurality of non-volatile multi-level memory cell, electric currents flowing through the channels of the multi-level memory cells of the first group and electric currents flowing through the channels of the multi-level memory cells of the second group being substantially flowing in a same

direction, a method of operating the electrically alterable non-volatile multi-level memory device, comprising:

settling a parameter of at least one non-volatile multi-level memory cell of the plurality of non-volatile multi-level memory cells to one state selected from a plurality of states including at least a first state, a second state, a third state and a fourth state in response to information to be stored in the one non-volatile multi-level memory cell,

verifying whether the parameter of the one non-volatile multi-level memory cell has being settled to the one state selected from the plurality of states by comparing the parameter of the one non-volatile multi-level memory cell with a plurality of verifying reference parameters including at least a first verifying reference parameter, a second verifying reference parameter, a third verifying reference parameter and a fourth verifying reference parameter, and of repeating the operation for settling the parameter and the operation for verifying until it is verified by the operation for verifying that the parameter of the one non-volatile multi-level memory cell has being settled to the one state,

reading status of the one non-volatile multi-level memory cell by comparing the parameter with a plurality of reading reference parameters including at least a first reading reference parameter, a second reading reference parameter and a third reading reference parameter,

wherein a conductivity value of the one non-volatile multi-level memory cell is decreased in order of the first state, the second state, the third state and the fourth state,

wherein the first reading reference parameter is allocated between the first state and the second state, the second reading reference parameter is allocated between the second state and the third state, and the third reading reference parameter is allocated between the third state and the fourth state,

wherein the first reading reference parameter, the second reading reference parameter and the third reading reference parameter are parameters for a normal read operation in which the information stored in the one non-volatile multi-level memory cell can be read out by output data of a plurality of bits,

wherein the normal read operation is carried out by parallel-comparing the parameter with the plurality of reading reference parameters by using a plurality of sense circuits including at least a first sense circuit, a second sense circuit and a third sense circuit, first input terminals of the first sense circuit, the second sense circuit and the third sense circuit are commonly supplied with the parameter from the one non-volatile multi-level memory cell, a second input terminal of the first sense circuit is supplied with the first reading reference parameter, a second input terminal of the second sense circuit is supplied with the second reading reference parameter and a second input terminal of the third sense circuit is supplied with the third reading reference parameter, and

wherein the first verifying reference parameter is allocated below the first reading reference parameter, the second verifying reference parameter is allocated between the first reading reference parameter and the second reading reference parameter, the third verifying reference parameter is allocated between the second reading reference parameter and the third reading reference parameter and the fourth verifying reference parameter is allocated above the third reading reference parameter.

As claim 63 of the present application is a direct copy of the proposed Count 1, it so corresponds.

(3) Claim Chart for the Count

Section (3) requires a claim chart for the proposed count comparing at least one claim of each party showing why they interfere within the meaning of Sec. 41.203(a).

As the proposed Count 1 is Claim 63 of the present application, they correspond exactly:

Claim 63 of Present Application	Count 1
For an electrically alterable non-volatile multi-level memory device including a plurality of non-volatile multi-level memory cells, each of the multi-level memory cells including a floating gate FET having a channel with electrically alterable voltage threshold value, the plurality of non-volatile multi-level memory cells being disposed in a matrix of rows and columns, channels of multi-level memory cells of a first group of the plurality of non-volatile multi-level memory cells being coupled in parallel between a first bit line and a reference potential, channels of multi-level memory cells of a second group of the plurality of non-volatile multi-level memory cells being coupled in parallel between a second bit line and the reference potential, electrons being capable of being injected into the floating gate from the channel of each of the plurality of non-volatile multi-level memory cell, electric currents flowing through the channels of the multi-level memory cells of the first group and electric currents flowing through the channels of the	For an electrically alterable non-volatile multi-level memory device including a plurality of non-volatile multi-level memory cells, each of the multi-level memory cells including a floating gate FET having a channel with electrically alterable voltage threshold value, the plurality of non-volatile multi-level memory cells being disposed in a matrix of rows and columns, channels of multi-level memory cells of a first group of the plurality of non-volatile multi-level memory cells being coupled in parallel between a first bit line and a reference potential, channels of multi-level memory cells of a second group of the plurality of non-volatile multi-level memory cells being coupled in parallel between a second bit line and the reference potential, electrons being capable of being injected into the floating gate from the channel of each of the plurality of non-volatile multi-level memory cell, electric currents flowing through the channels of the multi-level memory cells of the first group and electric currents flowing through the channels of the

multi-level memory cells of the second group being substantially flowing in a same direction, a method of operating the electrically alterable non-volatile multi-level memory device, comprising:	multi-level memory cells of the second group being substantially flowing in a same direction, a method of operating the electrically alterable non-volatile multi-level memory device, comprising:
settling a parameter of at least one non-volatile multi-level memory cell of the plurality of non-volatile multi-level memory cells to one state selected from a plurality of states including at least a first state, a second state, a third state and a fourth state in response to information to be stored in the one non-volatile multi-level memory cell,	settling a parameter of at least one non-volatile multi-level memory cell of the plurality of non-volatile multi-level memory cells to one state selected from a plurality of states including at least a first state, a second state, a third state and a fourth state in response to information to be stored in the one non-volatile multi-level memory cell,
verifying whether the parameter of the one non-volatile multi-level memory cell has being settled to the one state selected from the plurality of states by comparing the parameter of the one non-volatile multi-level memory cell with a plurality of verifying reference parameters including at least a first verifying reference parameter, a second verifying reference parameter, a third verifying reference parameter and a fourth verifying reference parameter, and of repeating the operation for settling the parameter and the operation for verifying until it is verified by the operation for verifying that the parameter of the one non-volatile multi-level memory cell has being settled to the one state,	verifying whether the parameter of the one non-volatile multi-level memory cell has being settled to the one state selected from the plurality of states by comparing the parameter of the one non-volatile multi-level memory cell with a plurality of verifying reference parameters including at least a first verifying reference parameter, a second verifying reference parameter, a third verifying reference parameter and a fourth verifying reference parameter, and of repeating the operation for settling the parameter and the operation for verifying until it is verified by the operation for verifying that the parameter of the one non-volatile multi-level memory cell has being settled to the one state,

reading status of the one non-volatile multi-level memory cell by comparing the parameter with a plurality of reading reference parameters including at least a first reading reference parameter, a second reading reference parameter and a third reading reference parameter, .	reading status of the one non-volatile multi-level memory cell by comparing the parameter with a plurality of reading reference parameters including at least a first reading reference parameter, a second reading reference parameter and a third reading reference parameter, .
wherein a conductivity value of the one non-volatile multi-level memory cell is decreased in order of the first state, the second state, the third state and the fourth state,	wherein a conductivity value of the one non-volatile multi-level memory cell is decreased in order of the first state, the second state, the third state and the fourth state,
wherein the first reading reference parameter is allocated between the first state and the second state, the second reading reference parameter is allocated between the second state and the third state, and the third reading reference parameter is allocated between the third state and the fourth state,	wherein the first reading reference parameter is allocated between the first state and the second state, the second reading reference parameter is allocated between the second state and the third state, and the third reading reference parameter is allocated between the third state and the fourth state,
wherein the first reading reference parameter, the second reading reference parameter and the third reading reference parameter are parameters for a normal read operation in which the information stored in the one non-volatile multi-level memory cell can be read out by output data of a plurality of bits,	wherein the first reading reference parameter, the second reading reference parameter and the third reading reference parameter are parameters for a normal read operation in which the information stored in the one non-volatile multi-level memory cell can be read out by output data of a plurality of bits,
wherein the normal read operation is carried out by parallel-comparing the parameter with the plurality of reading	wherein the normal read operation is carried out by parallel-comparing the parameter with the plurality of reading

reference parameters by using a plurality of sense circuits including at least a first sense circuit, a second sense circuit and a third sense circuit, first input terminals of the first sense circuit, the second sense circuit and the third sense circuit are commonly supplied with the parameter from the one non-volatile multi-level memory cell, a second input terminal of the first sense circuit is supplied with the first reading reference parameter, a second input terminal of the second sense circuit is supplied with the second reading reference parameter and a second input terminal of the third sense circuit is supplied with the third reading reference parameter, and	reference parameters by using a plurality of sense circuits including at least a first sense circuit, a second sense circuit and a third sense circuit, first input terminals of the first sense circuit, the second sense circuit and the third sense circuit are commonly supplied with the parameter from the one non-volatile multi-level memory cell, a second input terminal of the first sense circuit is supplied with the first reading reference parameter, a second input terminal of the second sense circuit is supplied with the second reading reference parameter and a second input terminal of the third sense circuit is supplied with the third reading reference parameter, and
wherein the first verifying reference parameter is allocated below the first reading reference parameter, the second verifying reference parameter is allocated between the first reading reference parameter and the second reading reference parameter, the third verifying reference parameter is allocated between the second reading reference parameter and the third reading reference parameter and the fourth verifying reference parameter is allocated above the third reading reference parameter.	wherein the first verifying reference parameter is allocated below the first reading reference parameter, the second verifying reference parameter is allocated between the first reading reference parameter and the second reading reference parameter, the third verifying reference parameter is allocated between the second reading reference parameter and the third reading reference parameter and the fourth verifying reference parameter is allocated above the third reading reference parameter.

As the proposed Count 1 differs from the claim 1 of U.S. patent number 6,014,327only in the preamble specifying a specific electron injection mechanism (hot electron injection), which does not enter into the claim elements, they also correspond:

Claim 1 of U.S. patent number 6,014,327	Count 1
For an electrically alterable non-volatile multi-level memory device including a plurality of non-volatile multi-level memory cells, each of the multi-level memory cells including a floating gate FET having a channel with electrically alterable voltage threshold value, the plurality of non-volatile multi-level memory cells being disposed in a matrix of rows and columns, channels of multi-level memory cells of a first group of the plurality of non-volatile multi-level memory cells being coupled in parallel between a first bit line and a reference potential, channels of multi-level memory cells of a second group of the plurality of non-volatile multi-level memory cells being coupled in parallel between a second bit line and the reference potential, electrons being capable of being injected into the floating gate by a phenomenon of hot electron injection from the channel of each of the plurality of non-volatile multi-level memory cell, electric currents flowing through the channels of the multi-level memory cells of the first group and electric currents flowing through the channels of the	For an electrically alterable non-volatile multi-level memory device including a plurality of non-volatile multi-level memory cells, each of the multi-level memory cells including a floating gate FET having a channel with electrically alterable voltage threshold value, the plurality of non-volatile multi-level memory cells being disposed in a matrix of rows and columns, channels of multi-level memory cells of a first group of the plurality of non-volatile multi-level memory cells being coupled in parallel between a first bit line and a reference potential, channels of multi-level memory cells of a second group of the plurality of non-volatile multi-level memory cells being coupled in parallel between a second bit line and the reference potential, electrons being capable of being injected into the floating gate from the channel of each of the plurality of non-volatile multi-level memory cell, electric currents flowing through the channels of the multi-level memory cells of the first group and electric currents flowing through the channels of the multi-level memory cells of the second group

multi-level memory cells of the second group being substantially flowing in a same direction, a method of operating the electrically alterable non-volatile multi-level memory device, comprising:	being substantially flowing in a same direction, a method of operating the electrically alterable non-volatile multi-level memory device, comprising:
settling a parameter of at least one non-volatile multi-level memory cell of the plurality of non-volatile multi-level memory cells to one state selected from a plurality of states including at least a first state, a second state, a third state and a fourth state in response to information to be stored in the one non-volatile multi-level memory cell,	settling a parameter of at least one non-volatile multi-level memory cell of the plurality of non-volatile multi-level memory cells to one state selected from a plurality of states including at least a first state, a second state, a third state and a fourth state in response to information to be stored in the one non-volatile multi-level memory cell,
verifying whether the parameter of the one non-volatile multi-level memory cell has being settled to the one state selected from the plurality of states by comparing the parameter of the one non-volatile multi-level memory cell with a plurality of verifying reference parameters including at least a first verifying reference parameter, a second verifying reference parameter, a third verifying reference parameter and a fourth verifying reference parameter, and of repeating the operation for settling the parameter and the operation for verifying until it is verified by the operation for verifying that the parameter of the one non-volatile multi-level memory cell has being settled to the one state,	verifying whether the parameter of the one non-volatile multi-level memory cell has being settled to the one state selected from the plurality of states by comparing the parameter of the one non-volatile multi-level memory cell with a plurality of verifying reference parameters including at least a first verifying reference parameter, a second verifying reference parameter, a third verifying reference parameter and a fourth verifying reference parameter, and of repeating the operation for settling the parameter and the operation for verifying until it is verified by the operation for verifying that the parameter of the one non-volatile multi-level memory cell has being settled to the one state,

reading status of the one non-volatile multi-level memory cell by comparing the parameter with a plurality of reading reference parameters including at least a first reading reference parameter, a second reading reference parameter and a third reading reference parameter, .	reading status of the one non-volatile multi-level memory cell by comparing the parameter with a plurality of reading reference parameters including at least a first reading reference parameter, a second reading reference parameter and a third reading reference parameter, .
wherein a conductivity value of the one non-volatile multi-level memory cell is decreased in order of the first state, the second state, the third state and the fourth state,	wherein a conductivity value of the one non-volatile multi-level memory cell is decreased in order of the first state, the second state, the third state and the fourth state,
wherein the first reading reference parameter is allocated between the first state and the second state, the second reading reference parameter is allocated between the second state and the third state, and the third reading reference parameter is allocated between the third state and the fourth state,	wherein the first reading reference parameter is allocated between the first state and the second state, the second reading reference parameter is allocated between the second state and the third state, and the third reading reference parameter is allocated between the third state and the fourth state,
wherein the first reading reference parameter, the second reading reference parameter and the third reading reference parameter are parameters for a normal read operation in which the information stored in the one non-volatile multi-level memory cell can be read out by output data of a plurality of bits,	wherein the first reading reference parameter, the second reading reference parameter and the third reading reference parameter are parameters for a normal read operation in which the information stored in the one non-volatile multi-level memory cell can be read out by output data of a plurality of bits,
wherein the normal read operation is carried out by parallel-comparing the parameter with the plurality of reading	wherein the normal read operation is carried out by parallel-comparing the parameter with the plurality of reading

reference parameters by using a plurality of sense circuits including at least a first sense circuit, a second sense circuit and a third sense circuit, first input terminals of the first sense circuit, the second sense circuit and the third sense circuit are commonly supplied with the parameter from the one non-volatile multi-level memory cell, a second input terminal of the first sense circuit is supplied with the first reading reference parameter, a second input terminal of the second sense circuit is supplied with the second reading reference parameter and a second input terminal of the third sense circuit is supplied with the third reading reference parameter, and	reference parameters by using a plurality of sense circuits including at least a first sense circuit, a second sense circuit and a third sense circuit, first input terminals of the first sense circuit, the second sense circuit and the third sense circuit are commonly supplied with the parameter from the one non-volatile multi-level memory cell, a second input terminal of the first sense circuit is supplied with the first reading reference parameter, a second input terminal of the second sense circuit is supplied with the second reading reference parameter and a second input terminal of the third sense circuit is supplied with the third reading reference parameter, and
wherein the first verifying reference parameter is allocated below the first reading reference parameter, the second verifying reference parameter is allocated between the first reading reference parameter and the second reading reference parameter, the third verifying reference parameter is allocated between the second reading reference parameter and the third reading reference parameter and the fourth verifying reference parameter is allocated above the third reading reference parameter.	wherein the first verifying reference parameter is allocated below the first reading reference parameter, the second verifying reference parameter is allocated between the first reading reference parameter and the second reading reference parameter, the third verifying reference parameter is allocated between the second reading reference parameter and the third reading reference parameter and the fourth verifying reference parameter is allocated above the third reading reference parameter.

As the claims correspond and the present application will prevail on priority, as described in the next section, the claims interfere within the meaning of Sec. 41.203(a).

(4) How Applicant Will prevail on Priority

Section (4) requires an explanation of why the applicant will prevail on priority.

As specified in the "Cross-Reference to Related Application" section added to the beginning of the present application by Preliminary Amendment filed concurrently with the present application, and as is also shown on the filing receipt, the present application is a continuation of U.S. patent application serial number 09/188,417, filed on November 9, 1998, now U.S. patent number 6,304,485, which is which is a continuation of U.S. patent application serial number 08/771,708, filed on December 20, 1996, now U.S. patent number 5,991,517, which is in turn a continuation of U.S. patent application serial number 08/174,768, filed on December 29, 1993, now U.S. patent number 5,602,987, which is in turn a continuation of U.S. patent application serial number 07/963,838, filed on October 20, 1992, now U.S. patent number 5,297,148, which is a division of U.S. patent application serial number 07/337,566, filed on April 13, 1989, now abandoned. Consequently, the present application is entitled to an effective filing date of April 13, 1989.

U.S. patent 6,014,327 of Banks has a filing date of May 14, 1999, and claiming priority from a number of U.S. patent applications (in one case through a continuation in-part), the earliest of which has a filing date of February 8, 1991. Thus, this earliest priority date is well over a year after the priority date to which the present application is entitled.

Similarly, U.S. patent 6,356,486 of Banks has a filing date of June 5, 2000, and claiming priority from a number of U.S. patent applications, the earliest of which has a filing date of February 8, 1991. Thus, this earliest priority date is well over a year after the priority date to which the present application is entitled.

Similarly, U.S. patent 6,381,172 of Banks has a filing date of May 14, 1999, and claiming priority from a number of U.S. patent applications (in one case through a continuation in-part), the earliest of which has a filing date of February 27, 1995. Thus, this earliest priority date is several years after the priority date to which the present application is entitled

Similarly, U.S. patent 6,404,675of Banks has a filing date of June 11, 2002, and claiming priority from a number of U.S. patent applications, the earliest of which has a filing date of February 8, 1991. Thus, this earliest priority date is well over a year after the priority date to which the present application is entitled

(5,6) Claim Charts

The following claim charts are as previously submitted. They show the corresponding written description for each claim in the specification of the present application. They also show where the disclosure provides a constructive reduction to practice within the scope of the interfering subject matter.

Support for Claims

Pending Claims	Present Application
63. For an electrically alterable non-volatile multi-level memory device including a plurality of non-volatile multi-level memory cells, each of the multi-level memory cells including a floating gate FET having a channel with electrically alterable voltage threshold value, the plurality of non-volatile multi-level memory cells being disposed in a matrix of rows and columns, channels of multi-level memory cells of a first group of the plurality of non-volatile multi-level memory cells being coupled in parallel between a first bit line and a reference potential, channels of multi-level memory cells of a second group of the plurality of non-volatile multi-level memory cells being coupled in parallel between a second bit line and the reference potential, electrons being capable of being injected into the floating gate from the channel of each of the plurality of non-volatile multi-level memory cell, electric currents flowing through the channels of the multi-level memory cells of the first group and electric currents flowing through the channels of the multi-level memory cells of the second group being substantially flowing in a same direction, a method of operating the electrically alterable non-volatile multi-level memory device, comprising:	All of the exemplary embodiments are multi-level non-volatile, floating gate FET memory cells. Exemplary array structures with the described matrix structure are shown in Figures 15a and 15b of `344 and Figures 12 and 22 of the present application.  The injection mechanism is described briefly at column 1, lines 42-47, of `344 and in more detail for various cell embodiments beginning at column 5, line 33. See also page 11, lines 18-19 of Preliminary Amendment.

settling a parameter of at least one non-volatile multi-level memory cell of the plurality of non-volatile multi-level memory cells to one state selected from a plurality of states including at least a first state, a second state, a third state and a fourth state in response to information to be stored in the one non-volatile multi-level memory cell,	"Settling" is the program pulse, column 25, lines 16-20, of `344, and step 6 of Figure 23 of the present application. The states are shown in terms of threshold voltage in Figure 15A of the present application. See also Figure 11c of `344 for the current-voltage relation of the states, which is the same as Figure 15B of the present application.
verifying whether the parameter of the one non-volatile multi-level memory cell has being settled to the one state selected from the plurality of states by comparing the parameter of the one non-volatile multi-level memory cell with a plurality of verifying reference parameters including at least a first verifying reference parameter, a second verifying reference parameter, a third verifying reference parameter and a fourth verifying reference parameter, and of repeating the operation for settling the parameter and the operation for verifying until it is verified by the operation for verifying that the parameter of the one non-volatile multi-level memory cell has being settled to the one state,	See column 26, lines 18-35, of `344. Also, steps 4 and 5 of Figure 23 of the present application.  See also Figures 11c and 11e of `344 for the verifying reference parameters (the I_{REF}s) and the corresponding circuitry. Column 25, lines 16-20, of `338. Also, the "repeating the operation…" corresponds to the loop of steps 4, 5, and 6 of Figure 23 of the present application.
reading status of the one non-volatile multi-level memory cell by comparing the parameter with a plurality of reading reference parameters including at least a first	See again Figures 11c and 11e of `344 and the corresponding description beginning at line 34 of column 26 for the reading reference parameters (the I_{DS}s) and

reading reference parameter, a second reading reference parameter and a third reading reference parameter, .	the corresponding circuitry. See also page 12, starting at line 6, of the Preliminary Amendment.
wherein a conductivity value of the one non-volatile multi-level memory cell is decreased in order of the first state, the second state, the third state and the fourth state,	Figures 11c of `338 and 15A and 15B of the present application.
wherein the first reading reference parameter is allocated between the first state and the second state, the second reading reference parameter is allocated between the second state and the third state, and the third reading reference parameter is allocated between the third state and the fourth state,	Figures 11c and 11e and column 26, lines 36-65, of `344.
wherein the first reading reference parameter, the second reading reference parameter and the third reading reference parameter are parameters for a normal read operation in which the information stored in the one non-volatile multi-level memory cell can be read out by output data of a plurality of bits,	See again Figures 11c and 11e of `344 and the corresponding description beginning at column 26, lines 36-65, of `344.
wherein the normal read operation is carried out by parallel-comparing the parameter with the plurality of reading reference parameters by using a plurality of sense circuits including at least a first sense circuit, a second sense circuit and a third sense circuit, first input terminals of the first	Figure 11e of `344 and column 26, lines 4-17 and 39-42. The sense circuits (SENSE AMPs) are commonly connected in parallel to the BIT LINE and receive the respective reference currents.

sense circuit, the second sense circuit and the third sense circuit are commonly supplied with the parameter from the one non-volatile multi-level memory cell, a second input terminal of the first sense circuit is supplied with the first reading reference parameter, a second input terminal of the second sense circuit is supplied with the second reading reference parameter and a second input terminal of the third sense circuit is supplied with the third reading reference parameter, and	
wherein the first verifying reference parameter is allocated below the first reading reference parameter, the second verifying reference parameter is allocated between the first reading reference parameter and the second reading reference parameter, the third verifying reference parameter is allocated between the second reading reference parameter and the third reading reference parameter and the fourth verifying reference parameter is allocated above the third reading reference parameter.	The relation of the verifying reference parameters and the reading reference parameters is described in `344, column 26, lines 51-65.

64. The method of operating the electrically alterable non-volatile multi-level memory according to claim 63, wherein the operation for settling the parameter includes a program operation in which electrons are	As noted above, the "settling the parameter" is a program operation. Electrons being injected into the floating gate is standard Flash memory operation; see, for example, column 1, lines 20-28, of `344.

injected into a floating gate of the one non-volatile multi-level memory cell.	

Claims 65 and 66 differ from claims 63 and 64, respectively, in the replacement of "a parameter" with "an electrical value" and in the replacement of "settling a parameter" with "controlling an electrical value". As noted above in the support for claim 63, the "parameter" can be taken as the threshold voltage and the "settling" or "controlling" is the application of a programming pulse. Consequently, the support for claims 65 and 66 is respectively the same as that for 63 and 64 and will not be repeated to save space.

Claims 67 and 68 are device claims that directly correspond, respectively, to method claims 63 and 64 on an element by element basis. Consequently, the support for claims 67 and 68 is again respectively the same as that for 63 and 64 and will also not be repeated to save space.

69. The electrically alterable non-volatile multi-level memory according to claim 68, further comprising, a plurality of bit lines, including said first and said second bit line, each of which transfers information indicating data stored in a memory cell, wherein drain regions of said multi-level memory cells of said first group in said matrix are coupled to said first bit line of said plurality of bit lines, drain regions of said multi-level memory cells of said second group adjoining to said first group in said matrix are coupled to said second bit line adjoining to said first bit line in said plurality	The described matrix structure is shown in Figures 15a and 15b of `344 and Figures 12 and 22 of the present application.

of bit lines and drain regions of multi-level memory cells of a third group adjoining to said second column in said matrix are coupled to a third bit line adjoining to said second bit line in said plurality of bit lines.	

Claims 70-72 differ from claims 67-69, respectively, in the replacement of "a parameter" with "an electrical value" and in the replacement of "settling a parameter" with "controlling an electrical value". As noted above in the support for claim 63, the "parameter" can be taken as the threshold voltage and the "settling" or "controlling" is the application of a programming pulse. Consequently, the support for claims 70-72 is respectively the same as that for 67-69 and will not be repeated to save space.

73. An electrically non-volatile multi-level memory device comprising:	The exemplary embodiments are all electrical non-volatile multi-level memory devices
a plurality of memory cells disposed in matrix having rows and columns,	Figures 12 and 22 of the present application and Figures 15a and 15b of `344.
wherein each of said plurality of memory cells has a threshold voltage corresponding to data of two bits,	Figures 11c of `344 and 15A and 15B of the present application.
wherein threshold voltages of said plurality of memory cells are allocated to one of a first, a second, a third and a fourth threshold range,	Figures 11c of `344 and 15A and 15B of the present application.
wherein said first threshold range indicates an erase state, and said second, said third, said fourth threshold range indicate program states different from said erase state,	Figures 11c of `344 and 15A and 15B of the present application.
wherein said second, said third and	Figures 11c of `344 and 15A and 15B

said fourth threshold range indicate mutually different programming states,	of the present application.
wherein a threshold voltage of a memory cell selected from said plurality of memory cells is allocated in one of said first, said second and said third threshold range, and	Figures 11c of `344 and 15A and 15B of the present application.
wherein control gates of memory cells on the same row in said matrix are coupled to a word line of a plurality of word lines,	Figures 12 and 22 of the present application and Figures 15a and 15b of `344.
a plurality of bit lines each of which transfers information indicating data stored in a memory cell, wherein drain regions of memory cells on a first column in said matrix are coupled to a first bit line of said plurality of bit lines, drain regions of memory cells on a second column adjoining to said first column in said matrix are coupled to a second bit line adjoining to said first bit line in said plurality of bit lines and drain regions of memory cells on a third column adjoining to said second column in said matrix are coupled to a third bit line adjoining to said second bit line in said plurality of bit lines,	Figures 12 and 22 of the present application and Figures 15a and 15b of `344.
a programming circuit programming ones of said plurality of memory cells to said programming states by using verify reference parameters,	Figure 11e of `344: programming control, bit line and word line progr. pulse. See Figure 22 of the present application
a sense circuit which compares information indicating data stored in a	Figure 11e, lower left portion, and column 26, lines 51-65, of `344.

memory cell with a first reference parameter, a second reference parameter and a third reference parameter in parallel, in a normal read operation,	
wherein said first threshold range is lower than said second threshold range, said second threshold range is lower than said third threshold range, and said third threshold range is lower than said fourth threshold range,	Figure 11c and column 26, lines 51-65, of `344 and Figures 15A and 15B of the present application.
wherein said third reference parameter is higher than said second reference parameter, and said second reference parameter is higher than said first reference parameter,	Figure 11c and column 26, lines 51-65, of `344 and Figures 15A and 15B of the present application.
wherein said verify reference parameters have at least first and second verify reference parameters,	Figure 11c and column 26, lines 51-65, of `344 and Figures 15A and 15B of the present application.
wherein said first verify reference parameter is allocated between said second threshold range and said third threshold range, and said second verify reference parameter is allocated between said first threshold range and said second threshold range, and	Figure 11c and column 26, lines 51-65, of `344 and Figures 15A and 15B of the present application.
wherein said first verify reference parameter is settled between said second reference parameter and said third reference parameter, and said second verify reference parameter is settled between said first	Figure 11c and column 26, lines 51-65, of `344 and Figures 15A and 15B of the present application.

reference parameter and said second reference parameter.	
74. An electrically non-volatile multi-level memory device according to claim 73, wherein each of said plurality of memory cells has a floating gate, and a threshold voltage of a selected memory cell is allocated to one of said first, said second and said third threshold range from said fourth threshold range by being injected with hot electron to a floating gate of said selected memory cell.	For floating gate, see Figures 9-11 of the present application. The threshold voltages are shown in Figures 15A and 15B of the present application. Hot electron injection is specified in `344 at column 27, line 53, column 5, line 67, and column 10, line 62.
75. An electrically non-volatile multi-level memory device according to claim 74, further comprising, a column select circuit which receives column addresses, and which couples selected bit lines to said sense circuits.	1101, 1107,and 1109 of Figure 12, of the present application. Sense circuits1220 are shown in Figure 13.
76. An electrically non-volatile multi-level memory device according to claim 75, wherein each of said sense circuits has a first comparator which receives said information and said first reference parameter, a second comparator which receives said information and said second reference parameter and a third comparator which receives said information and said third reference	Figure 11e, lower left portion, and column 26, lines 51-65, of `344.

parameter.	

77. An electrically non-volatile multi-level memory device according to claim 75, wherein each of said plurality of memory cells has a source region to which is supplied with a reference potential in said read operation.	Figure 12 of the present application. Source region is denoted "S" and reference potential is "V_S", where exemplary values are given in Tables 1 and 2 of Figures 26 and 27.

80. For an electrically alterable non-volatile multi-level semiconductor memory device including a plurality of non-volatile multi-level memory cells, each of the multi-level memory cells including a floating gate FET having a channel with electrically alterable voltage threshold value, the plurality of non-volatile multi-level memory cells being disposed in a matrix of rows and columns, channels of multi-level memory cells of a group of the plurality of non-volatile multi-level memory cells being coupled in parallel between a bit line and a reference potential, electrons being capable of being injected into the floating gate from the channel in each of the plurality of non-volatile multi-level memory cells, a method of operating the electrically alterable non-volatile multi-level semiconductor memory device, comprising:	All of the exemplary embodiments are multi-level non-volatile, floating gate FET memory cells. Exemplary array structures with the described matrix structure are shown in Figures 15a and 15b of `344 and Figures 12 and 22 of the present application.  The injection mechanism is described briefly at column 1, lines 42-47, of `344 and in more detail for various cell embodiments beginning at column 5, line 33. See also page 11, lines 18-19 of Preliminary Amendment.

setting a parameter of at least one non-volatile multi-level memory cell of the plurality of non-volatile multi-level memory cells to a state selected from a plurality of states including at least a first state, a second state, a third state and a fourth state in response to information to be stored in the one non-volatile multi-level memory cell,	Setting is the program pulse, column 25, lines 16-20, of `344, and step 6 of Figure 23 of the present application. The states are shown in terms of threshold voltage in Figure 15A of the present application. See also Figure 11c of `344 for the current-voltage relation of the states, which is the same as Figure 15B of the present application.
when one of the first third states is selected, verifying whether the parameter of the one non-volatile multi-level memory cell has been set to the one state, including comparing the parameter of the one non-volatile multi-level memory cell with one of a plurality of verifying reference parameters including at least a first verifying reference parameter, a second verifying reference parameter and a third verifying reference parameter, the operation of setting the parameter being conducted until it is verified by the operation of verifying that the parameter of the one non-volatile multi-level memory cell has been set to the one state,	See column 26, lines 18-35, of `344. Also, steps 4 and 5 of Figure 23 of the present application.  See also Figures 11c and 11e of `344 for the verifying reference parameters (the I_{REF}s) and the corresponding circuitry. Column 25, lines 16-20, of `344. Also, the "repeating the operation…" corresponds to the loop of steps 4, 5, and 6 of Figure 23 of the present application.
reading status of the one non-volatile multi-level memory cell, including comparing the parameter of the one non-volatile multi-level memory cell, with a plurality of reading reference parameters including at least a first reading reference parameter, a second reading reference	See again Figures 11c and 11e of `344 and the corresponding description beginning at line 34 of column 26 for the reading reference parameters (the I_{DS}s) and the corresponding circuitry. See also page 12, starting at line 6, of the Preliminary Amendment.

parameter and a third reading reference parameter,	
wherein a conductivity value of the one non-volatile multi-level memory cell is increased in order of the first state, the second state, the third state and the fourth state,	Figures 11c of `344 and 15A and 15B of the present application.
wherein the first reading reference parameter is allocated between the first state and the second state, the second reading reference parameter is allocated between the second state and the third state, and the third reading reference parameter is allocated between the third state and the fourth state,	Figures 11c and 11e and column 26, lines 36-65, of `344.
wherein the first reading reference parameter, the second reading reference parameter and the third reading reference parameter are parameters for a normal read operation in which the information stored in the one non-volatile multi-level memory cell can be read out as output data of a plurality of bits,	See again Figures 11c and 11e of `344 and the corresponding description beginning at column 26, lines 36-65, of `344.
wherein the normal read operation includes parallel-comparing the parameter of the one non-volatile multi-level memory cell with the plurality of reading reference parameters using a plurality of sense circuits including at least a first sense circuit, a second sense circuit and a third sense circuit, first input terminals of the first sense circuit, the second sense circuit and the third sense	Figure 11e of `344 and column 26, lines 4-17. The sense circuits (SENSE AMPs) are commonly connected in parallel to the BIT LINE and receive the respective reference currents.

circuit are commonly supplied with the parameter of the one non-volatile multi-level memory cell, a second input terminal of the first sense circuit is supplied with the first reading reference parameter, a second input terminal of the second sense circuit is supplied with the second reading reference parameter and a second input terminal of the third sense circuit is supplied with the third reading reference parameter,	
wherein the first verifying reference parameter is allocated above the first reading reference parameter, the second verifying reference parameter is allocated between the first reading reference parameter and the second reading reference parameter and the third verifying reference parameter is allocated between the second reading reference parameter and the third reading reference parameter, and	The relation of the verifying reference parameters and the reading reference parameters is described in `344, column 26, lines 51-65.
wherein the plurality of non-volatile multi-level memory cells of the matrix of the rows and the columns are disposed, in substantially a rectangle that has a first side, a second side, a third side and a fourth side, the first side and the second side intersect with each other substantially perpendicularly, a plurality of word lines coupled with gate electrodes of floating gate FET's of the multi-level memory cells and the first side of the	The described matrix structure is shown in Figures 15a and 15b of `344 and Figures 12 and 22 of the present application.

rectangle intersect with each other substantially perpendicularly, a plurality of bit lines coupled with drains of floating gate FET's of the multi-level memory cells and the second side of the rectangle intersect with each other substantially perpendicularly, a row select circuit is disposed at the first side of the rectangle for coupling with the plurality of word lines, and peripheral circuitry, including a column select circuit, sense circuits, a data conversion circuit and latches, is disposed at the second side of the rectangle.	

81. The method of operating the electrically alterable non-volatile multi-level memory according to claim 80, wherein the operation of setting the parameter includes an erasure operation in which non-volatile multi-level memory cells of one of a byte, a block and a chip level can be erased.	Figure 23, step (1), of the present application shows the erase operation as an initial step in the programming.

82. The method of operating the electrically alterable non-volatile multi-level memory according to claim 81, wherein the operation of setting the parameter includes a program operation in which electrons are injected into a floating gate of the one non-volatile multi-level	Figure 23, steps (4)-(6), of the present application.

memory cell.	

Claims 83-85 differ from claims 80-82, respectively, in the replacement of “a parameter” with “an electrical value” and in the replacement of “setting a parameter” with “controlling an electrical value”. As noted above in the support for claim 80, the “parameter” can be taken as the threshold voltage and the “setting” or “controlling” is the application of a programming pulse. Consequently, the support for claims 83-85 is respectively the same as that for 80-82 and will not be repeated to save space.

Claims 86-88 are device claims that directly correspond, respectively, to method claims 80-82 on an element by element basis. Consequently, the support for claims 86-88 is again respectively the same as that for 80-82 and will also not be repeated to save space.

89. The electrically alterable non-volatile multi-level memory according to claim 88,	
wherein each of the plurality of bit lines transfers information indicating data stored in a memory cell, wherein drain regions of said multi-level memory cells of said group in said matrix are coupled to a first bit line of said plurality of bit lines, drain regions of multi-level memory cells of a second group adjacent to said group in said matrix are coupled to a second bit line adjacent to said first bit line in said plurality of bit lines and drain regions of multi-level memory cells of a third group adjacent to said second group in said matrix are coupled to a third bit line adjacent to said second bit line in said plurality of bit lines.	The described matrix structure is shown in Figures 15a and 15b of `344 and Figures 12 and 22 of the present application.

Claims 90-93 differ from claims 86-89, respectively, in the replacement of "a parameter" with "an electrical value" and in the replacement of "setting a parameter" with "controlling an electrical value". As noted above in the support for claim 80, the "parameter" can be taken as the threshold voltage and the "settling" or "controlling" is the application of a programming pulse. Consequently, the support for claims 90-93 is respectively the same as that for 86-89 and will not be repeated to save space.

94. A non-volatile semiconductor memory device comprising:	The exemplary embodiments are all non-volatile semiconductor memory devices.
a plurality of non-volatile memory cells each of which has a threshold voltage representing data of at least two bits, wherein threshold voltages of the plurality of non-volatile memory cells are shiftable among at least three threshold levels which indicate mutually different programming states and which also differ from a threshold level indicating an erase state;	Figures 12 and 22 of the present application and Figures 15a and 15b of `344. Figure 11c and column 26, lines 51-65, of `344 and Figures 15A and 15B of the present application.
parameter generating circuitry generating a first programming reference parameter, a first read reference parameter, a second programming reference parameter, a second read reference parameter, a third programming reference parameter and a third read reference parameter; and	One embodiment uses the reference cells of Figure 17B of the present application.
sensing/program-verifying circuitry receiving a parameter which represents threshold voltage of one non-volatile memory cell, the first programming reference parameter, the first read reference parameter,	1440 of Figure 17B of the present application; Figure 11e, lower left portion, and column 26, lines 51-65, of `344.

the second programming reference parameter, the second read reference parameter, the third programming reference parameter and the third read reference parameter;	
wherein the first read reference parameter is allocated between a level corresponding to the erase state and the first programming reference parameter, the second read reference parameter is allocated between the first programming reference parameter and the second programming reference parameter, and the third read reference parameter is allocated between the second programming reference parameter and the third programming reference parameter,	Figure 11c and column 26, lines 51-65, of `344 and Figures 15A and 15B of the present application.
wherein the sensing/program-verifying circuitry generates data of at least two bits represented by the one non-volatile memory cell threshold voltage, verifies whether the one non-volatile memory cell threshold voltage is shifted to the threshold level indicating a selected one of the programming states, and programs the one non-volatile memory cell until it is verified that the one non-volatile memory cell threshold voltage has been shifted to that threshold level,	Figure 17B of the present application; Figure 11e, lower left portion, and column 26, lines 51-65, of `344. A program algorithm is shown in Figure 23 of the present application.
wherein the first programming reference parameter is used for verifying whether non-volatile memory cell threshold	Figure 11c and column 26, lines 51-65, of `344 and Figures 15A and 15B of the present application.

voltages are shifted to a first threshold level of the three threshold levels, the first read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the first threshold level or to the threshold level indicating the erase state, and one of the first programming reference parameter and the first read reference parameter is shifted from and dependent upon the other,	`344, column 26, lines 60-65: "shifted by a fixed amount …"
wherein the second programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a second threshold level of the three threshold levels, the second read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the second threshold level or to the first threshold level, and one of the second programming reference parameter and the second read reference parameter is shifted from and dependent upon the other, and	Figure 11c and column 26, lines 51-65, of `344 and Figures 15A and 15B of the present application. `344, column 26, lines 60-65: "shifted by a fixed amount …"
wherein the third programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a third threshold level of the three threshold levels, the third read reference parameter is used for detecting whether non-volatile memory cell threshold	Figure 11c and column 26, lines 51-65, of `344 and Figures 15A and 15B of the present application.

voltages are near to the third threshold level or to the second threshold level, and one of the third programming reference parameter and the third read reference parameter is shifted from and dependent upon the other.	`344, column 26, lines 60-65: "shifted by a fixed amount …"

95. A non-volatile semiconductor memory device according to claim 94, wherein the parameter generating circuitry includes a first parameter generating circuit which generates the first programming reference parameter and the first read reference parameter, a second parameter generating circuit which generates the second programming reference parameter and the second read reference parameter, and a third parameter generating circuit which generates the third programming reference parameter and the third read reference parameter, and	The reference cells of Figure 17B of the present application.
wherein each of the first parameter generating circuit, the second parameter generating circuit and the third parameter generating circuit includes an element causing the corresponding one reference parameter and the corresponding other reference parameter to have different values.	The reference cells of Figure 17B of the present application.

96. A non-volatile semiconductor memory device according to claim 95, wherein each of the first parameter	

generating circuit, the second parameter generating circuit and the third parameter generating circuit further includes a reference cell which has substantially the same construction as each of said plurality of memory cells, and the reference cell and the element of each parameter generating circuit cooperate to provide a predetermined difference between the corresponding read and programming reference parameters.	The reference cells of Figure 17B of the present application.

97. A non-volatile semiconductor memory device according to claim 94, wherein each read reference parameter is dependent upon the corresponding programming reference parameter.	`344, column 26, lines 60-65: "shifted by a fixed amount ..."

98. A non-volatile semiconductor memory device according to claim 94, wherein a conductivity value of the one non-volatile memory cell is decreased in order of the threshold level indicating the erase state, the first threshold level, the second threshold level and the third threshold level, and	Figure 11c of `344 and Figures 15A and 15B of the present application.
wherein threshold voltages of non-volatile memory cells of one of a byte, a block and a chip level can be shifted to the threshold level indicating the erase state by	See the "Erase of Memory Structures" section, beginning on page 8, line 6, and Figure 2 of the present application.

an erase operation.	

99. A non-volatile semiconductor memory device according to claim 98,	
wherein each of the plurality of non-volatile memory cells has a floating gate to which electrons are capable of being injected from a channel.	Figures 9-11 of the present application.

Aside from differing in the claim upon which they depend, claims 100, 102, 104, and 109 are the same as claim 98. Similarly, claims 101, 103, 105 and 110 are the same as claim 99, except for a change of dependence. Therefore, the support for claims 100, 102, 104, and 109 and claims 101, 103, 105 and 110 is the same as that given above for claim 98 and claim 99, respectively, and will not be repeated in order to same space.

106. A non-volatile semiconductor memory device according to claim 94,	
wherein the first, second and third read reference parameters are dependent upon the first, second and third programming reference parameters, respectively.	`344, column 26, lines 60-65: "shifted by a fixed amount …"

107. A non-volatile semiconductor memory device comprising:	The exemplary embodiments are all non-volatile semiconductor memory devices.
a plurality of non-volatile memory cells each of which has a floating gate and a threshold voltage representing data of at least two bits, wherein electrons are capable of being injected into the floating gate, and wherein threshold voltages of the plurality of	Figures 12 and 22 of the present application and Figures 15a and 15b of `344. Figure 11c and column 26, lines 51-65, of `344 and Figures 15A and 15B of the present application.

non-volatile memory cells are shiftable among at least three threshold levels which indicate mutually different programming states and which also differ from a threshold level indicating an erase state; and	
sensing/program-verifying circuitry receiving a parameter which represents the threshold voltage of one non-volatile memory cell, a first programming reference parameter, a first read reference parameter, a second programming reference parameter, a second read reference parameter, a third programming reference parameter and a third read reference parameter;	1440 of Figure 17B of the present application; Figure 11e, lower left portion, and column 26, lines 51-65, of `344.
wherein the first read reference parameter is allocated to represent a level between the threshold level indicating the erase state and a level represented by the first programming reference parameter, the second read reference parameter is allocated between the first programming reference parameter and the second programming reference parameter, and the third read reference parameter is allocated between the second programming reference parameter and the third programming reference parameter,	Figure 11c and column 26, lines 51-65, of `344 and Figures 15A and 15B of the present application.
wherein the sensing/program-verifying circuitry generates data of at least two bits represented by the one non-volatile memory cell threshold voltage, verifies	Figure 17B of the present application; Figure 11e, lower left portion, and column 26, lines 51-65, of `344. A program algorithm is shown in Figure 23 of the

whether the one non-volatile memory cell threshold voltage is shifted to the threshold level indicating a selected one of the programming states, and programs the one non-volatile memory cell until it is verified that the one non-volatile memory cell threshold voltage has been shifted to that threshold level,	present application.
wherein the first programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a first threshold level of the three threshold levels, and the first read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the first threshold level or to the threshold level indicating the erase state,	Figure 11c and column 26, lines 51-65, of `344 and Figures 15A and 15B of the present application.
wherein the second programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a second threshold level of the three threshold levels, and the second read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the second threshold level or to the first threshold level,	Figure 11c and column 26, lines 51-65, of `344 and Figures 15A and 15B of the present application.
wherein the third programming reference parameter is used for verifying whether non-volatile memory cell threshold	Figure 11c and column 26, lines 51-65, of `344 and Figures 15A and 15B of the present application.

voltages are shifted to a third threshold level of the three threshold levels, and the third read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the third threshold level or to the second threshold level,	
wherein the first read reference parameter, the second read reference parameter and the third read reference parameter are parameters for a normal read operation in which the information stored in the one non-volatile memory cell can be read out as output data of a plurality of bits,	See again Figures 11c and 11e of `344 and the corresponding description beginning at column 26, lines 36-65, of `344.
wherein the normal read operation includes parallel-comparing the parameter representing the threshold voltage of the one non-volatile memory cell with the plurality of reading reference parameters using a plurality of sense circuits including at least a first sense circuit, a second sense circuit and a third sense circuit, first input terminals of the first sense circuit, the second sense circuit and the third sense circuit are commonly supplied with the parameter from the one non-volatile multi-level memory cell, a second input terminal of the first sense circuit is supplied with the first read reference parameter, a second input terminal of the second sense circuit is supplied with the second read reference parameter and a second	Figure 11e of `344 and column 26, lines 4-17 and 39-42. The sense circuits (SENSE AMPs) are commonly connected in parallel to the BIT LINE and receive the respective reference currents.

input terminal of the third sense circuit is supplied with the third read reference parameter,	
wherein the first read reference parameter is allocated to represent a level between the threshold level indicating the erase state and the first threshold level, the second read reference parameter is allocated to represent a level between the first threshold level and the second threshold level, and the third read reference parameter is allocated to represent a level between the second threshold level and the third threshold level, and	Figure 11c and column 26, lines 51-65, of `344 and Figures 15A and 15B of the present application.
wherein the level represented by the second read reference parameter is allocated substantially at a midpoint between the first threshold level and the second threshold level, and the level represented by the first read reference parameter is allocated toward the first threshold level from a midpoint between the threshold level indicating the erase state and the first threshold level.	On "midpoint", see `344, column 26, line 63: "to place them closer to the midpoint".

108. A non-volatile semiconductor memory device according to claim 107, wherein an operation of shifting the one non-volatile memory cell threshold voltage to the threshold level indicating the selected programming state includes a	Figure 11e of `344 (bit line and word line pulsing circuitry, waveforms) or Figure 23, steps (4)-(6) of the present application.

program operation in which electrons are injected into the floating gate of the one non-volatile memory cell by applying at least one programming pulse to a bit line coupled to a drain of the one non-volatile memory cell.	

Claims 109 and 111 are, aside from a difference in dependence, the same as claim 98. Similarly, aside from a difference in dependence, claims 110 and 112 are the same as claim 99. Consequently, support for these claims is provided above and will not be repeated.

113. A non-volatile semiconductor memory device comprising:	The exemplary embodiments are all non-volatile semiconductor memory devices.
a plurality of non-volatile memory cells each of which has a floating gate and a threshold voltage representing data of at least two bits, wherein electrons are capable of being injected into the floating gate, and wherein threshold voltages of the plurality of non-volatile memory cells are shiftable among at least three threshold levels which indicate mutually different programming states and which also differ from a threshold level indicating an erase state; and	Figures 12 and 22 of the present application and Figures 15a and 15b of `344. Figure 11c and column 26, lines 51-65, of `344 and Figures 15A and 15B of the present application.
sensing/program-verifying circuitry receiving a parameter which represents the threshold voltage of one non-volatile memory cell, a first programming reference parameter, a first read reference parameter, a second programming reference parameter, a second read reference parameter, a third	1440 of Figure 17B of the present application; Figure 11e, lower left portion, and column 26, lines 51-65, of `344.

programming reference parameter and a third read reference parameter;	
wherein the first read reference parameter is allocated to represent a level between the threshold level indicating the erase state and a level represented by the first programming reference parameter, the second read reference parameter is allocated between the first programming reference parameter and the second programming reference parameter, and the third read reference parameter is allocated between the second programming reference parameter and the third programming reference parameter,	Figure 11c and column 26, lines 51-65, of `344 and Figures 15A and 15B of the present application.
wherein the sensing/program-verifying circuitry generates data of at least two bits represented by the one non-volatile memory cell threshold voltage, verifies whether the one non-volatile memory cell threshold voltage is shifted to the threshold level indicating a selected one of the programming states, and programs the one non-volatile memory cell until it is verified that the one non-volatile memory cell threshold voltage has been shifted to that threshold level,	Figure 17B of the present application; Figure 11e, lower left portion, and column 26, lines 51-65, of `344. A program algorithm is shown in Figure 23 of the present application.
wherein the first programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a first threshold level	Figure 11c and column 26, lines 51-65, of `344 and Figures 15A and 15B of the present application.

of the three threshold levels, and the first read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the first threshold level or to the threshold level indicating the erase state,	
wherein the second programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a second threshold level of the three threshold levels, and the second read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the second threshold level or to the first threshold level,	Figure 11c and column 26, lines 51-65, of `344 and Figures 15A and 15B of the present application.
wherein the third programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a third threshold level of the three threshold levels, and the third read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the third threshold level or to the second threshold level,	Figure 11c and column 26, lines 51-65, of `344 and Figures 15A and 15B of the present application.
wherein the first read reference parameter, the second read reference parameter and the third read reference parameter are parameters for a normal read operation in which the information stored in the one non-volatile memory cell can be read	See again Figures 11c and 11e of `344 and the corresponding description beginning at column 26, lines 36-65, of `344.

out as output data of a plurality of bits,	
wherein the normal read operation includes parallel-comparing the parameter representing the threshold voltage of the one non-volatile memory cell with the plurality of reading reference parameters using a plurality of sense circuits including at least a first sense circuit, a second sense circuit and a third sense circuit, first input terminals of the first sense circuit, the second sense circuit and the third sense circuit are commonly supplied with the parameter representing the threshold voltage of the one non-volatile memory cell, a second input terminal of the first sense circuit is supplied with the first read reference parameter, a second input terminal of the second sense circuit is supplied with the second read reference parameter and a second input terminal of the third sense circuit is supplied with the third read reference parameter,	Figure 11e of `344 and column 26, lines 4-17 and 39-42. The sense circuits (SENSE AMPs) are commonly connected in parallel to the BIT LINE and receive the respective reference currents.
wherein the first read reference parameter is allocated to represent a level between the threshold level indicating the erase state and the first threshold level, the second read reference parameter is allocated to represent a level between the first threshold level and the second threshold level, and the third read reference parameter is allocated to represent a level between the	Figure 11c and column 26, lines 51-65, of `344 and Figures 15A and 15B of the present application.

second threshold level and the third threshold level, and	
wherein the level represented by the second read reference parameter is allocated substantially at a midpoint between the first threshold level and the second threshold level, and the level represented by the third read reference parameter is allocated toward the second threshold level from a midpoint between the second threshold level and the third threshold level.	Figure 11e of `344 (bit line and word line pulsing circuitry, waveforms) or Figure 23, steps (4)-(6) of the present application.

Claims 115 and 117 are, aside from a difference in dependence, the same as claim 109. Similarly, aside from a difference in dependence, claims 116 and 118 are the same as claim 110 and claim 114 is the same as claim 108. Consequently, support for these claims is provided above and will not be repeated.

119. A non-volatile semiconductor memory device …	Claim 119 is the same as 113 except for middle part of last element. See claim 113 above for the omitted elements.
wherein the level represented by the second read reference parameter is allocated substantially at a midpoint between the first threshold level and the second threshold level, and the level represented by the first read reference parameter is allocated toward the first threshold level from a midpoint between the threshold level indicating the erase state and the first threshold level, and the level represented by the third read	On "midpoint", see `344, column 26, line 63: "to place them closer to the midpoint"

reference parameter is allocated toward the second threshold level from a midpoint between the second threshold level and the third threshold level.	

Claims 121 and 123 are, aside from a difference in dependence, the same as claim 109. Similarly, aside from a difference in dependence, claims 122 and 124 are the same as claim 110 and claim 120 is the same as claim 108. Consequently, support for these claims is provided above and will not be repeated.

As presented above, it is respectfully submitted that the present application supports all of the currently pending claims and an early indication of their allowability is earnestly solicited. In the meantime, a phone call to the undersigned is invited should there be any questions.

Respectfully submitted,

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